REMARKS/ARGUMENTS

Claims 1-27 are pending. Claims 1-13 and 17-27 including independent claims 1, 17, and 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi (2002/0038401 A1) in view of Heinkle (2004/0015739 A1) in view of Whitten (5,805,795). Claims 25-27 were rejected as being directed to software per se. Applicants filed a Pre-appeal Brief Request For Review on January 31, 2008 and the arguments were accepted. Prosecution has been reopened and the Examiner set forth new grounds for rejecting the claims.

The Examiner rejected claims 25-27 under 35 U.S.C. 101 because the Examiner argues the claims are "software per se" and "invocation of U.S.C. 112(6) is invalidated." The Applicants respectfully disagree. The Applicants respectfully disagree that claims 25-27 are directed to software per se. Claims 25 recite "processing means" and "interface means." These means elements provide structural and functional interrelationships between functional elements and the rest of a system such as a computing processing system, provide a "useful, tangible, and concrete result" and are believed to be statutory. See State Street Bank v. Signature Financial Group. Furthermore, the invocation of USC 112(6) is not believed invalidated simply because the Specification states that "For example, various aspects described above may be implemented using firmware, software, or hardware. Aspects of the present invention may be employed with a variety of different file formats, languages, and communication protocols and should not be restricted to the ones mentioned above." The broadening language is not intended to claim everything, but instead merely states not every possible embodiment can be described. Furthermore, "means for" language pertaining to software is patentable and has sufficient structure if an "algorithm that transforms the general purpose microprocessor to a "special purpose computer programmed to perform the disclosed algorithm." See Aristocrat Technologies Australia v. International Gaming Technologies. Algorithms are provided throughout the present application, including Figure 5, 6, 7, and 8 and associated description.

The Examiner cites new grounds in rejecting claims 1-3, 5, 17-21, and 25-27. More specifically, the Examiner rejects the claims under 35 U.S.C. 103(a) as being unpatentable over Whitten (US 5,805,795) in view of Bening (Optimizing Multiple EDA Tools within the ASIC Design Flow).

The Examiner relies on Whitten to describe "selecting a plurality of submodules from a design module library" and "wherein a probabilististic function is applied to select submodules of different types from the library.

The Examiner argues that the claim recitation "selecting a plurality of submodules from a design module library" is taught or suggested by the Whitten description "It is assumed that a comprehensive complete collection of test cases has been initially generated or collected by a test designer, in a manner known in the art, to test the assertions made about the software, as described above. In the diagram of FIG. 2, the entire collection of test cases is made available in a list or collection 10." (column 4, line 64 – column 5, line 2) The Applicants respectfully disagree. Multiple test cases are not a plurality of submodules as recited in the claims. The specification explicitly describes submodules. "Possible submodules include memory modules 431 and 433, phase locked loop module 451, adder 453, filter 455, and timer 457. The top-level module 401 also includes registers 441, 443, 445, and 447. In this example, other submodules included in the top-level module 401 are DSP core 461, processor core 463, etc. Each submodule may also be associated with various input and output lines. The various input and output lines can be categorized as clock lines, control lines, or data lines." (page 12, lines 25-31). Furthermore, one of skill in the art would not interpret a plurality of submodules selected from a submodule library to mean multiple test cases, even if the claim terms are interpreted in their broadest possible scope. Test cases are not referred to as submodules. Test cases are not obtained from a submodule library. Neither intrinsic evidence nor extrinsic evidence supports an interpretation of submodule as a test case. If the Examiner maintains this rejection, it is respectfully requested that the Examiner provide even one or two references that define a submodule as a test case or a submodule library as a library of test cases.

Furthermore, dependent claims 7 and 8 recite submodule input lines and submodule output lines. If submodule is interpreted to mean test case, submodule input lines and submodule output lines would make no sense. Whitten software generated test cases do not have intput lines or output lines.

Nonetheless, to facilitate prosecution, claim 3 has been amended to facilitate prosecution. Claim 3 now recites "wherein the plurality of submodules comprise a memory module and a Digital Signal Processor (DSP) core." Whitten test cases are not memory modules or DSP cores and do not include memory modules or DSP cores.

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants believe that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
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